1 and 2-Watt MMIC Power Amplifiers for Commercial K/Ka-Band Applications

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Abstract — **Two ICs, specifically designed for commercial applications at K/Ka-band frequencies, are presented. These ICs provide 1 and 2 watts of linear power respectively, gain levels of typically 17 dB and a power added efficiency of 25% at the 1-dB gain compression point. While the RF performance parameters are not state-of-the-art, these compact chips establish new levels for power density, i.e. the ratio of output power to chip area. This figure of merit is particularly important for the cost sensitive commercial market.**

I. INTRODUCTION

Current and future commercial applications at K/Ka-band such as LMDS require low-cost linear power MMICs with output power levels of 1 watt or more [1]. While other parameters are certainly important, the key system specifications for such an amplifier are usually the output power at the 1-dB gain compression point, P_{1dB}, and the chip cost. It should be noted that P_{1dB}, while convenient, is not necessarily an accurate measure of the ability of the amplifier to handle multiple signals without generating spurious signals. A better measure is the third-order intercept point, IP3, or ACPR for digital modulation schemes.

While there are certainly other factors that influence the chip cost, the single most dominant factor is the chip area. Hence, an important figure of merit for linear power MMICs is the ratio of the P_{1dB} to the chip area. Chips with the largest figure of merit should provide the highest linear output power for the least dollars. It is the purpose of this paper to present two new ICs that were designed specifically for these commercial applications. These ICs establish new levels for this power-density figure of merit. While not producing state-of-the-art levels for the output power, bandwidth or efficiency, these chips exhibit competitive RF performance while utilizing very little GaAs real estate.

II. DESIGN APPROACH

the same design principles, and hence are very similar in design. As a consequence, only design information on the 2-watt IC is presented.

The 2-watt amplifier configuration is shown in Fig. 1. It consists of a 2-stage, power amplifier design with four 600 μm cells in the first stage driving eight 600 μm cells in the output stage. This 1-to-2 driver-to-output gate periphery ratio was chosen in order to minimize the first stage contribution to the output distortion. The 600 μm PHEMT cells were configured internally as six, 0.20 x 100 μm gate fingers.

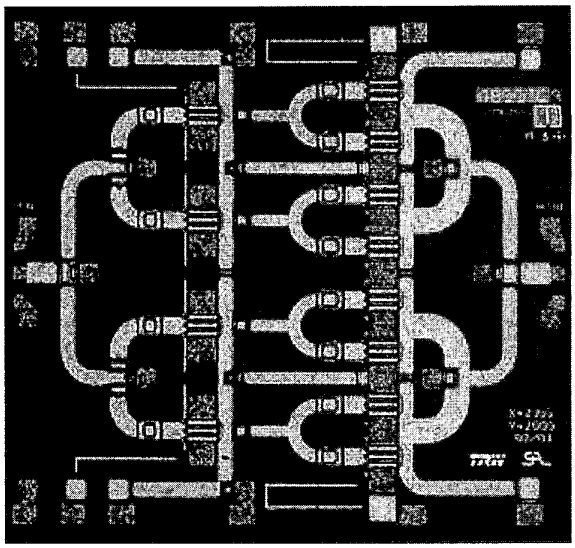

Fig. 1. Photograph of 2-watt IC (2.1 x 2.0 mm^2)

The circuit layout employs microstrip TL elements, MIM capacitors and thin-film resistors. Lossy matching techniques are used in the interstage and the input matching networks to simultaneously compensate for the 6 dB per octave device gain roll-up and perform the matching functions. Isolation resistors are employed to terminate odd-mode type instabilities. The resulting ICs

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In order to minimize the chip size, lowpass LCL matching networks are used for the input, interstage and output matching networks. These networks consist of series TLs and shunt discrete MIM capacitors in an LCL configuration.

The resulting chip dimensions are 2.1 x 1.2 mm^2 and 2.1 x 2.0 mm^2 for the 1-watt and 2-watt ICs respectively. This is smaller, by at least a factor of two, than conventional ICs of comparable power levels.

III. IC PERFORMANCE

The ICs reported in this paper were fabricated at TRW's GaAs IC foundry in Redondo Beach, CA. The PHEMT process and device parameters are described in [2,3].

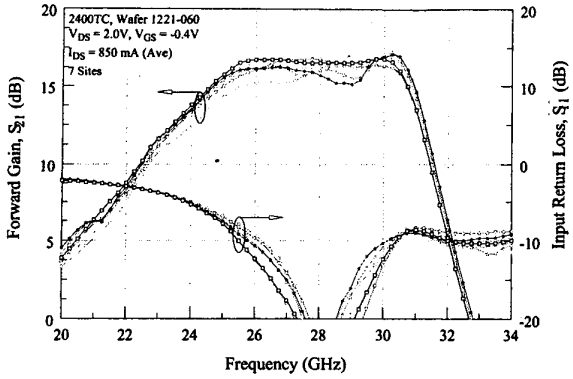

Fig. 2. On-Wafer, S-parameter Data for 1-Watt IC

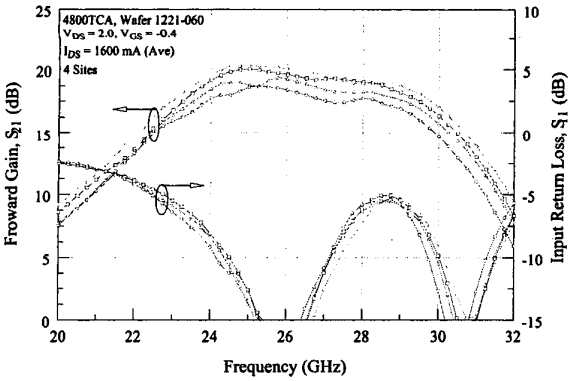

Fig. 3. On-Wafer, S-parameter Data for 2-Watt IC

For the small-signal measurements, the ICs were tested on-wafer with reduced drain bias to avoid thermal problems. The S-parameter data for the 1 and 2-watt ICs are shown in Figs. 2 and 3 respectively over the 20 to 34 GHz band. The 1-watt IC demonstrates a gain of typically 16 dB from 26 to 30 GHz, while the 2-watt IC exhibits a gain of 18 dB from 24 to 28 GHz. For these tests, the bias conditions were V_{DS} = 2V and V_{GS} = -0.4V.

For the power tests, we mounted several of these 1 and 2-watt chips in a hybrid test fixture which is similar to that shown in Fig. 4 of reference [4]. The measured back-to-back insertion loss of this test fixture is typically 1 dB at 30 GHz. The results reported below are corrected for this fixture loss.

The large-signal results for the 1-watt IC are summarized in Figs. 4 through 6. Fig. 4 shows the broadband output power as a function of frequency, over the 25 to 29 GHz band, with the input power as a parameter. For an input power of 10 dBm (near small signal), the output power exhibits a relatively flat (±1 dB) response across the 25 to 29 GHz band. With higher drive levels, the response shows uniform gain compression and some flattening, but no bandwidth distortion. With an input power level of 15 dBm, the output power is flat at 29.7 ± 0.42 dBm over the 25.25 to 29 GHz band.

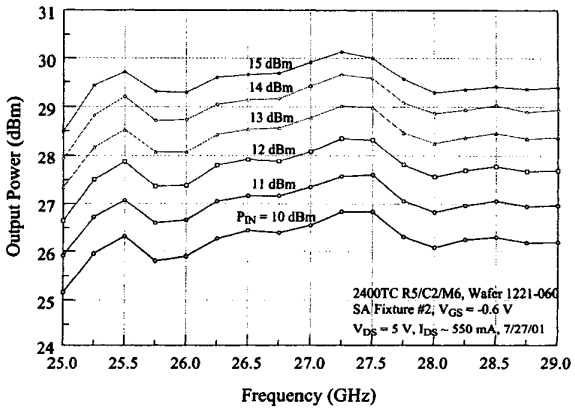

Fig. 4. Output Power as a Function of Frequency for the 1-Watt IC

The gain compression characteristics of this IC are shown in Fig. 5. This is plotted for V_{GS} = -0.6 V, V_{DS} = 5 V and five different frequencies ranging from 26.75 to 27.75 volts. As shown, P_{1dB} is typically 29 dBm.

The power performance of the IC at 27 GHz is summarized in Fig. 6. Again the bias conditions are V_{DS} = 5 V and V_{GS} = -0.6 V. This figure also shows the power-added efficiency and the drain bias current as a function of the drive level. At the 1-dB gain compression point, the output power is 29 dBm and the PAE is 24.9%.

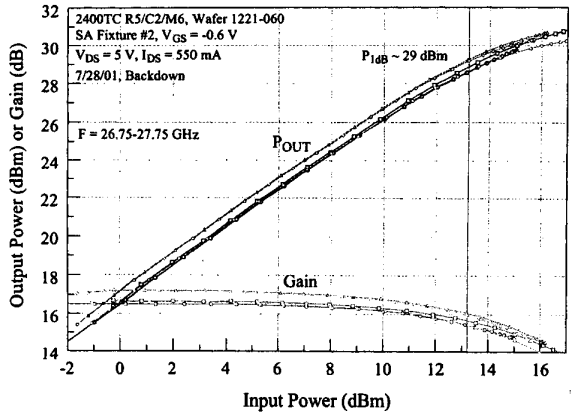

Fig. 5. Power Transfer Characteristics for the 1-Watt IC

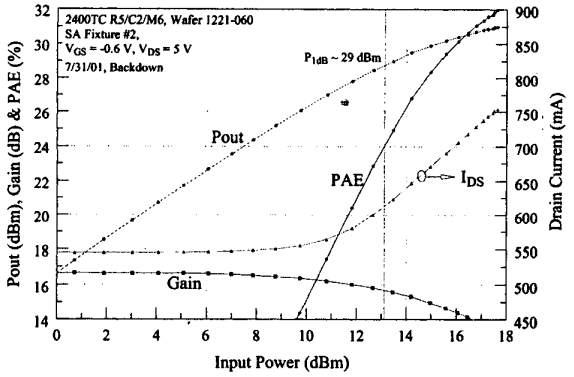

Fig. 6. Power Performance of 1-Watt IC at 27 GHz

The large-signal results for the 2-watt IC are summarized in Figs. 7 through 9. Fig. 7 shows the broadband output power as a function of frequency, over the 24 to 28 GHz band, with the input power as a parameter. The bias conditions for this test were V_{DS} = 5 V and V_{GS} = -0.6 V. For an input power of 10 dBm (near small signal), the output power exhibits a relatively flat (±1.5 dB) response across the 24 to 28 GHz band. With higher drive levels, the response shows uniform gain compression and some flattening, but no bandwidth distortion. With an input power level of 15 dBm, the output power level is greater than 32 dBm over the 24 to 26.5 GHz band.

The gain compression characteristics of this IC at 25 GHz are shown in Fig. 8. This is plotted for V_{GS} = -0.55 V and four different drain voltages ranging from 4 to 5.5 volts. As the IC is biased toward larger drain-source voltages, the gain-slope decreases and the output power at a specific gain compression point increases. Clearly, for best linear operation, we would want to bias this IC at or near V_{DS} = 5.5 V. At this bias point, P_{1dB} is 33.3 dBm (2.14 W).

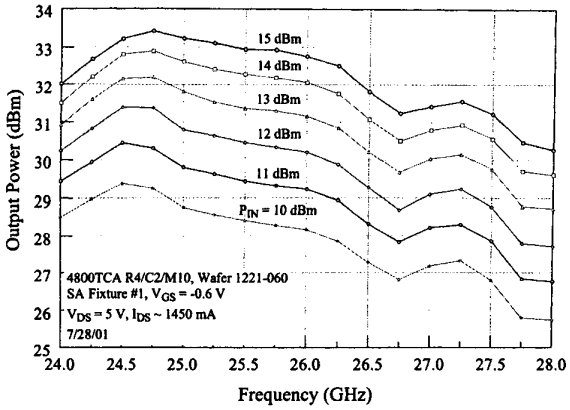

Fig. 7. Output Power versus Frequency for the 2-Watt IC

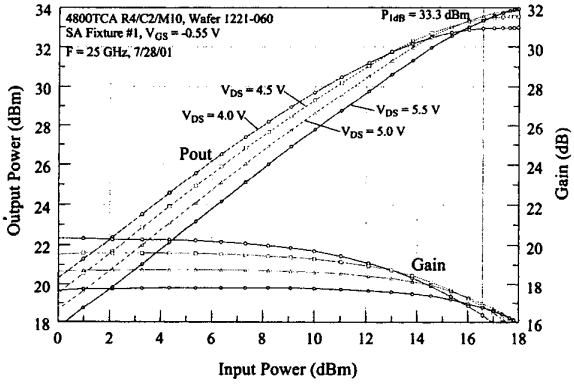

Fig. 8. Gain Compression Characteristics at 25 GHz for the 2-Watt IC

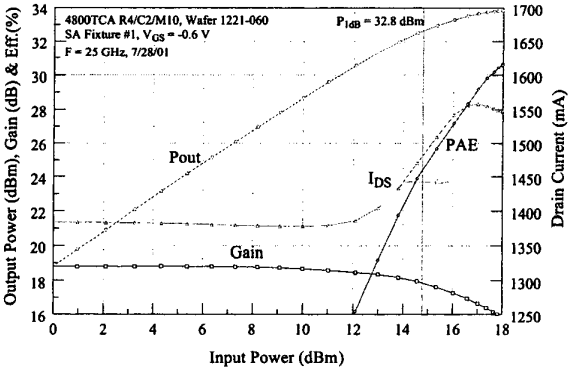

Fig. 9. Power Performance of 2-Watt IC at 25 GHz

Table I. Comparison of K/Ka-Band MMIC Power Amplifiers

P_{1dB} (W)	Freq (GHz)	1-dB BW (GHz)	Chip Area (mm^2)	Linear Gain (dB)	No. Stages	P_{OUT}/Area (W/mm^2)	Reference
1.26	29	3.5	15.1	17	2	0.083	[5]
1.26	30	2	12.1	16	2	0.10	[6]
3*	30	2	14.9	18	2	0.20	[7]
4**	30	2	26.3	22	3	0.15	[8]
1.79	30	2	11.99	17	3	0.15	[9]
0.79	27	9	3.91	14	2	0.20	[10]
0.79	29	4	3.69	16	3	0.22	[11]
0.79	27	4	2.52	17	2	0.31	This Work
2	25	2	4.20	18	2	0.48	This Work

*Pulsed result (25% duty), **Estimated based on P_{SAT} = 6 W

The power performance of the IC biased at V_{DS} = 5 V and V_{GS} = -0.6 V is shown in Fig. 9. This figure also shows the power-added efficiency and the drain bias current as a function of the drive level. At the 1-dB gain compression point, the output power is 32.8 dBm and the PAE is 25%.

Two-tone intermodulation tests at 25 GHz (not shown) indicate a 3rd-order intercept point (IP3) of 40.5 dBm. The bias conditions for these IM tests were V_{DS} = 5 V and V_{GS} = -0.6 V.

IV. Conclusion

We have presented two power MMICs specifically designed for commercial applications at K/Ka-band frequencies. These chips, with output power levels of 1 and 2 watts respectively, have demonstrated power densities (output power divided by the chip area) approaching 0.5 W/mm^2. Table I above puts these results into perspective. This table summarizes the performance of current K/Ka-band power MMICs either reported in the literature or available commercially. Only self contained (no hybrid assembles) MMICs with typically 17 dB small-signal gain (generally 2 stages) are included in this table. This table represents ICs with output power levels ranging from just under 1 watt to 4 watts. The output power density (column 7) ranges from a low of 0.083 to a high of 0.48. As shown, our best result ($0.48W/mm^2$) with the 2-watt IC is more than a factor of two larger than the previous best result. What this means practically is that, for the same output power, our chip is smaller than competing chips by a factor of two or more. All other things being equal, this should translate into a 2-to-1 cost advantage over completing ICs.

Acknowledgement

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